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DOCKET NO. 93-C-077C1 (STMI01-93077)
Customer No. 30425

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : LOI N. NGUYEN ET AL
U.S. Serial No. : 09/712,827
Filed : November 14, 2000
For : METHOD AND INTERLEVEL DIELECTRIC STRUCTURE FOR
IMPROVED METAL STEP COVERAGE
Group No. : 2814
Examiner : L. Pham

BOX AF
Commissioner for Patents
Washington, D.C. 20231

CERTIFICATE OF TRANSMISSION BY FACSIMILE

Sir:

The undersigned hereby certifies that the following documents:

1. Request for Clarification of Notice of Allowance

relating to the above application was faxed to 703-746-4082 on January 27, 2003.

Date: 1/27/03

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#13042
M. Braun
3/8/03

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Washington, D. C. 20231

Sir:

REQUEST FOR CLARIFICATION OF NOTICE OF ALLOWANCE

The Office Action mailed February 7, 2002 (Paper No. 8) and the Office Action mailed August 2, 2002 (Paper No. 10) indicates that claims 1 and 35-53 are pending in the subject application. However, the Notice of Allowability mailed on December 23, 2002 (Paper No. 12) identifies only claims 35-53 as being allowed, although claim 1 does not appear to have been cancelled by any amendment entered by either the Applicant or the Examiner. Clarification of the allowed claims is respectfully requested. A listing of the pending claims follows:

ATTORNEY DOCKET NO. STMI01-93077
U.S. SERIAL NO. 09/712,827
PATENT

PENDING CLAIMS

- 1 1. A fabrication method, comprising the steps of:
 - 2 forming a dielectric structure over a contact region, the dielectric structure comprising:
 - 3 a first layer formed from a first material; and
 - 4 a second layer overlying the first layer and formed from a second material which
 - 5 may be selectively etched with respect to the first material;
 - 6 forming and patterning a resist layer over the dielectric structure;
 - 7 selectively etching the second layer through an opening through the patterned resist layer
 - 8 utilizing an etch which is selective of the first material over the second material; and
 - 9 without stripping the resist layer, etching the dielectric structure through the opening
 - 10 within the patterned resist layer and any etched region within the second layer to form a contact
 - 11 opening extending through the dielectric structure and exposing the contact region.

ATTORNEY DOCKET NO. STMI01-93077
U.S. SERIAL NO. 09/712,827
PATENT

1 35. The method of claim 1, wherein the step of forming a dielectric structure over a contact
2 region further comprises:

3 forming a third layer underlying the first layer and formed from a material different than
4 the first material.

1 36. The method of claim 35, wherein the step of forming a dielectric structure over a contact
2 region further comprises:

3 forming a third layer from a silicate glass doped with a gettering agent;
4 forming the first layer of silicon nitride; and
5 forming the second layer of borophosphosilicate glass.

1 37. The method of claim 1, wherein the step of selectively etching the second layer through
2 an opening through the patterned resist layer utilizing an etch which is selective of the first
3 material over the second material further comprises:
4 etching an opening through the second layer.

ATTORNEY DOCKET NO. STMI01-93077
U.S. SERIAL NO. 09/712,827
PATENT

1 38. The method of claim 37, wherein the step of etching an opening through the second layer
2 further comprises:

3 utilizing a relatively isotropic etch process to etch the opening through the second layer,
4 wherein the opening through the second layer undercuts the patterned resist layer.

1 39. The method of claim 37, wherein the step of etching an opening through the second layer
2 further comprises:

3 utilizing a wet etch process to etch the opening through the second layer.

1 40. The method of claim 37, wherein the step of etching the dielectric structure through the
2 opening within the patterned resist layer and any etched region within the second layer to form
3 a contact opening extending through the dielectric structure and exposing the contact region
4 further comprises:

5 utilizing a relatively anisotropic etch process to etch a remainder of the opening
6 extending through the dielectric structure through the opening within the patterned resist layer.

ATTORNEY DOCKET NO. STMI01-93077
U.S. SERIAL NO. 09/712,827
PATENT

1 41. The method of claim 37, wherein the step of etching the dielectric structure through the
2 opening within the patterned resist layer and any etched region within the second layer to form
3 a contact opening extending through the dielectric structure and exposing the contact region
4 further comprises:

5 utilizing a plasma etch process to etch a remainder of the opening extending through the
6 dielectric structure through the opening within the patterned resist layer, the patterned resist
7 layer masking the plasma etch process.

ATTORNEY DOCKET NO. STMI01-93077
U.S. SERIAL NO. 09/712,827
PATENT

- 1 42. An intermediate integrated circuit structure, comprising:
2 a substrate including a contact region;
3 a dielectric structure over the substrate, the dielectric structure comprising:
4 a first layer formed from a first material; and
5 a second layer overlying the first layer and formed from a second material which
6 may be selectively etched with respect to the first material;
7 an opening through the dielectric structure and exposing the contact region, the opening
8 including
9 a first portion extending through the second layer having sloped or concave
10 sidewalls, and
11 a second portion extending through the first layer and having substantially
12 vertical sidewalls; and
13 a patterned resist layer overlying the dielectric structure, the patterned resist layer having
14 an opening therethrough over the opening through the dielectric structure.

ATTORNEY DOCKET NO. STMI01-93077
U.S. SERIAL NO. 09/712,827
PATENT

1 43. The intermediate integrated circuit structure of claim 43, wherein the dielectric structure
2 further comprises:
3 a third layer underlying the first layer and formed from a material different than the first
4 material.

1 44. The intermediate integrated circuit structure of claim 43, wherein the first layer is formed
2 of silicon nitride, the second layer is formed of borophosphosilicate glass, and the third layer
3 is formed of a silicate glass doped with a gettering agent.

1 45. The intermediate integrated circuit structure of claim 43, wherein the first portion of the
2 opening through the dielectric structure undercuts the patterned resist layer.

1 46. The intermediate integrated circuit structure of claim 43, wherein the opening through
2 the dielectric structure has a Y-shaped profile.

1 47. The intermediate integrated circuit structure of claim 43, wherein the opening through
2 the dielectric structure is wider within the first portion than the opening through the patterned
3 resist layer.

ATTORNEY DOCKET NO. STMI01-93077
U.S. SERIAL NO. 09/712,827
PATENT

1 48. The intermediate integrated circuit structure of claim 43, wherein the opening through
2 the dielectric structure has a width within the second portion approximately equal to a width of
3 the opening through the patterned resist layer.

1 49. A method of forming a contact opening, comprising:
2 forming a dielectric structure over a contact region, the dielectric structure comprising:
3 a first layer formed from a first material; and
4 a second layer overlying the first layer and formed from a second material which
5 may be selectively etched with respect to the first material;
6 forming and patterning a resist layer over the dielectric structure;
7 selectively etching the second layer through an opening through the patterned resist layer
8 utilizing a relatively isotropic etch process which is selective of the first material over the
9 second material and which undercuts the patterned resist layer in an etched region formed by
10 the relatively isotropic etch process; and
11 without stripping the resist layer, etching the dielectric structure, utilizing a relatively
12 anisotropic etch process, through the opening within the patterned resist layer and the etched
13 region within the second layer to form a contact opening extending through the dielectric
14 structure and exposing the contact region.

ATTORNEY DOCKET NO. STMI01-93077
U.S. SERIAL NO. 09/712,827
PATENT

1 50. The method of claim 49, wherein the step of selectively etching the second layer through
2 an opening through the patterned resist layer utilizing a relatively isotropic etch process which
3 is selective of the first material over the second material and which undercuts the patterned
4 resist layer in an etched region formed by the relatively isotropic etch process further comprises:
5 etching an opening through the second layer utilizing the first layer as an etch stop.

1 51. The method of claim 50, wherein the step of selectively etching the second layer through
2 an opening through the patterned resist layer utilizing a relatively isotropic etch process which
3 is selective of the first material over the second material and which undercuts the patterned
4 resist layer in an etched region formed by the relatively isotropic etch process further comprises:
5 wet etching the opening through the second layer utilizing hydrofluoric acid, wherein the
6 second layer is formed of a borophosphosilicate glass.

ATTORNEY DOCKET NO. STM101-93077
U.S. SERIAL NO. 09/712,827
PATENT

1 52. The method of claim 50, wherein the step of etching the dielectric structure, utilizing a
2 relatively anisotropic etch process, through the opening within the patterned resist layer and the
3 etched region within the second layer to form a contact opening extending through the dielectric
4 structure and exposing the contact region further comprises:

5 plasma etching a remainder of the opening through the dielectric structure through the
6 opening through the patterned resist layer and through the opening through the second layer.

1 53. The method of claim 52, wherein the step of plasma etching a remainder of the opening
2 through the dielectric structure through the opening through the patterned resist layer and
3 through the opening through the second layer further comprises:

4 masking the plasma etching process with the patterned resist layer.

ATTORNEY DOCKET NO. STMI01-93077
U.S. SERIAL NO. 09/712,827
PATENT


If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: 1-27-03


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